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10/680,592	10/07/2003	Christophe Pierrat	23748-10030	5273

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EXAMINER
GARBOWSKI, LEIGH M

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/680,592	**Applicant(s)** PIERRAT ET AL.
	Examiner Leigh Marie Garbowski	**Art Unit** 2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.
4a) Of the above claim(s) *32-55* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-31* is/are rejected.
7)☒ Claim(s) *5 and 14* is/are objected to.
8)☒ Claim(s) *1-55* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *(5 sheets)*. 10/07/2003, 09/06/2005, 10/17/2005
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-31, drawn to obtaining a layout description, verifying, and identifying weak spots, classified in class 716, subclass 4.

II. Claims 32-33, drawn to defining a physical connection, classified in class 716, subclass 12.

III. Claims 34-35, drawn to compacting a layout, classified in class 716, subclass 2.

IV. Claims 36-37, drawn to layout synthesis, classified in class 716, subclass 18.

V. Claims 38-39, drawn to generating a design rule, classified in class 716, subclass 5.

VI. Claims 40-41, drawn to extracting an electrical parameter, classified in class 716, subclass 5.

VII. Claims 42-46, drawn to interactive layout editing, classified in class 716, subclass 11.

VIII. Claims 47-51, drawn to modifying a layout, classified in class 716, subclass 11.

IX. Claims 52-53, drawn to disposing of an anomaly, classified in class 716, subclass 4.

X. Claims 54-55, drawn to manufacturing an IC, classified in class 716, subclass 19.

The inventions are distinct, each from the other because of the following reasons:

Inventions I through X are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as defining a physical connection of placed cells; invention III has separate utility such as compaction; invention IV has separate utility such as layout synthesis with a netlist; invention V has separate utility such as generating a design rule; invention VI has separate utility such as extraction; invention VII has separate utility such as interactive layout editing supplying feedback; invention VIII has separate utility such as modifying a layout; invention IX has separate utility such as disposing of an anomaly of a fabricated mask; and invention X has separate utility such as manufacturing an IC. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Search and examination of the entire application cannot be made without serious burden given the independent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Rajiv Patel on 11/03/2005 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-31. Affirmation of this election must be made by applicant in replying to this Office action. Claims 32-55 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "1294" [figure 12] and "1394" [figure 13] have both been used to designate "Unified model". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: what is meant by "the unified model, together with its associated manufacturing parameters (1302) and electrical parameters (1303)" [page 25, lines 19-20] is confusing, ish't the unified model comprised of elements 1302 and 1303 as per figure 13?. As page 30, line 5, "17bb" should be --17bb--. At paragraph [00114], the references to figures 18a through 18c should be corrected to accurately reflect each particular figure.

Appropriate correction is required.

Claim Objections

Claims 5 and 14 are objected to because of the following informalities: --of-- should be inserted after "representations" [line 2] to clarify the subject matter. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Taking claim 15 as exemplary of claims 15 and 17, what is meant by "said description is obtained by ..." is confusing since claim 10 recites how a description is computed [lines 10-11]; it is not clear from the language how the present features relate to those already established, thus rendering the claim confusing, vague and indefinite.

Claim 19 provides for the use of "a tolerance" [line 1], but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

As per claims 16, 18 and 20-22, although not specifically mentioned, the claims are rejected based on incorporating the error of their respective base claim by dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Smith et al. [U.S. Patent Application Publication #2003/0229875 A1].

As per claim 1, a method comprising: providing a layout of said target patterned layer [0132, 0138]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [0111], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [0111]; and computing a description of a portion of said layout using said first and said second parametric representation [0132, 0138]. As per claim 2, wherein said computing includes determining effects due to placement fluctuations, process variations, or a combination of both [0137]. As per claim 3, wherein said model is based on one of the following: physical theory, approximation, heuristics, or any combination thereof [0132]. As per claim 4, wherein said description includes one of the following: a physical description, an electrical description, or a combination of both [0132]. As per claim 5, wherein at least one of said parametric representations is one of the following parametric representations of: a lithography process, a mask-making process, an oxidation process, a deposition process, an etching process, an epitaxy process, an ion implantation process, a thermal process, a CMP process, a transistor, a capacitor, an inductor, or a resistor [0133, 0138]. As per claim 6, wherein said computing includes decomposition of said layout [0135]. As per claim 7, wherein said computing includes modification of said layout [0135]. As per claim 8, wherein said computing includes identification of a circuit element with said layout [0135]. As per claim 9, wherein said identification includes identification based on a physical description computed by said model [0135, 0137].

As per claim 10, a method comprising: providing a layout of said target patterned layer [0132, 0138]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [0111], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [0111]; computing a target description of a portion of said layout using said target patterned layer of material [0138]; computing a description of a portion of said layout using said first and said second parametric representation [0132, 0138]; and comparing said description with said target description [0138]. As per claim 11, wherein said computing includes determining effects due to placement fluctuations, process variations, or a combination of both [0137]. As per claim 12, wherein said description is checked against a design rule defined by the manufacturing and electrical requirements of said IC [0012, 0138]. As per claim 13, wherein said model is based on one of the following: physical theory, approximation, heuristics, or any combination thereof [0132]. As per claim 14, wherein at least one of said parametric representations is one of the following parametric representations of: a lithography process, a mask-making process, an oxidation process, a deposition process, an etching process, an epitaxy process, an ion implantation process, a thermal process, a CMP process, a transistor, a capacitor, an inductor, or a resistor [0133, 0138]. As per claims 15-18, wherein said modifying includes one of the following: dummy fill insertion, phase-shifting conversion, OPC, or any combination thereof [0029]. As per claims 19-23, wherein said comparing comprises: computing a difference between said description and said target description; and comparing said difference with said tolerance [0012, 0138]. As per claim 24, wherein said tolerance is determined using an electrical description determined by: identifying a circuit element with said layout; and obtaining said electrical description from said circuit element [0012, 0114]. As per claim 25, wherein said identifying comprises: decomposing said layout to obtain a decomposed geometry; and recognizing said circuit element with said decomposed geometry [0114]. As per claim 26, wherein said description and said target description includes manufacturing and electrical specifications [0111]. As per claim 27, wherein said manufacturing and electrical specification include one of the following: modulation transfer function, contrast, exposure latitude, image log slope, normalized image log slope, depth of focus, exposure-defocus window, total window, sensitivity to mask critical dimension error, sensitivity of aberrations, common window, linewidth variability, threshold voltage, leakage current, breakdown electric field, channel-length-modulation parameter, input and output impedance, input and output capacitance, input and output inductance, current density, current gain, unity current gain frequency, or any combination thereof [0029, 0112, 0138].

As per claim 28, a method comprising: providing a layout of said target patterned layer [0132, 0138]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [0111], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [0111]; providing a parameter of said model [0112]; providing a first and second value of said parameter of said model [0112]; computing a first description of a portion of said layout using said first value of said parameter, said first parametric representation, and said second parametric representation [0111, 0132, 0138]; computing a second description of a portion of said layout using said second value of said parameter, said first parametric representation, and said second parametric representation [0111, 0132, 0138]; comparing said first description and said second description [0138]. As per claim

29, wherein said comparing uses a design rule defined by the manufacturing and electrical requirements of said IC [0012, 0138].

As per claim 30, a method comprising: providing a layout of said target patterned layer [0132, 0138]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [0111], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [0111]; providing a parameter of said model [0112]; providing a first and second value of said parameter of said model [0112]; computing a first description of a portion of said layout using said first value of said parameter, said first parametric representation, and said second parametric representation [0111, 0132, 0138]; performing a first verification based on said first description and said target patterned layer, obtaining a first result [0114, 0138]; computing a second description of a portion of said layout using said second value of said parameter, said first parametric representation, and said second parametric representation [0111, 0132, 0138]; performing a second verification based on said second description and said target patterned layer, obtaining a second result [0114, 0138]; and comparing said first result with said second result [0138]. As per claim 31, wherein said comparing uses a design rule defined by the manufacturing and electrical requirements of said IC [0012, 0138].

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al. [U.S. Patent #6,904,587 B2].

As per claim 1, a method comprising: providing a layout of said target patterned layer [column 4, lines 63-66]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [column 10, lines 45-49], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [column 10, lines 49-53]; and computing a description of a portion of said layout using said first and said second parametric representation [column 5, lines 27-49]. As per claim 2, wherein said computing includes determining effects due to placement fluctuations, process variations, or a combination of both [column 1, lines 13-

20]. As per claim 3, wherein said model is based on one of the following: physical theory, approximation, heuristics, or any combination thereof [column 10, lines 45-57]. As per claim 4, wherein said description includes one of the following: a physical description, an electrical description, or a combination of both [column 10, lines 45-57]. As per claim 5, wherein at least one of said parametric representations is one of the following parametric representations of: a lithography process, a mask-making process, an oxidation process, a deposition process, an etching process, an epitaxy process, an ion implantation process, a thermal process, a CMP process, a transistor, a capacitor, an inductor, or a resistor [column 10, lines 45-57]. As per claim 6, wherein said computing includes decomposition of said layout [column 4, lines 31-47]. As per claim 7, wherein said computing includes modification of said layout [column 4, lines 48-53]. As per claim 8, wherein said computing includes identification of a circuit element with said layout [column 4, lines 24-31]. As per claim 9, wherein said identification includes identification based on a physical description computed by said model [column 4, lines 18-23].

As per claim 10, a method comprising: providing a layout of said target patterned layer [column 4, lines 63-66]; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer [column 10, lines 45-49], and a second parametric representation characterizing at least features of the IC dependent on one of the plurality of patterned layers other than the target patterned layer [column 10, lines 49-53]; computing a target description of a portion of said layout using said target patterned layer of material [column 4, lines 64-66]; computing a description of a portion of said layout using said first and said second parametric representation [column 5, lines 27-49]; and comparing said description with said target description [column 5, lines 27-48]. As per claim 11, wherein said computing includes determining effects due to placement fluctuations, process variations, or a combination of both [column 1, lines 13-20]. As per claim 12, wherein said description is checked against a design rule defined by the manufacturing and electrical requirements of said IC [column 5, lines 29-45]. As per claim 13, wherein said model is based on one of the following: physical theory, approximation, heuristics, or any combination thereof [column 10, lines 45-57]. As per claim 14, wherein at least one of said parametric representations is one of the following parametric representations of: a lithography process, a mask-making process, an oxidation process, a deposition process, an etching process, an epitaxy process, an ion implantation process, a thermal process, a CMP process, a transistor, a capacitor, an inductor, or a resistor [column 10, lines 45-57]. As per claims 15-18, wherein said modifying includes one of the following: dummy fill insertion, phase-shifting conversion, OPC, or any combination thereof [column 5, lines 8-21]. As per claims 19-23, wherein said comparing comprises: computing a difference between said description and said target description; and comparing said difference with said tolerance [column 5, lines 27-45]. As per claim 24, wherein said tolerance is determined using an electrical description determined by: identifying a circuit element with said layout; and obtaining said electrical description from said circuit element [column 5, lines 27-45]. As per claim 25, wherein said identifying comprises: decomposing said layout to obtain a decomposed geometry; and recognizing said circuit element with said decomposed geometry [column 4, lines 31-47]. As per claim 26, wherein said description and said target description includes manufacturing and electrical specifications [column 10, lines 46-57]. As per claim 27, wherein said manufacturing and electrical specification include one of the following: modulation transfer function, contrast, exposure latitude, image log slope, normalized image log slope, depth of focus, exposure-defocus window, total window, sensitivity to mask critical dimension error, sensitivity of aberrations, common window, linewidth variability, threshold voltage, leakage current, breakdown electric field, channel-length-modulation parameter, input and output impedance, input and output capacitance, input and output inductance, current density, current gain, unity current gain frequency, or any combination thereof [column 10, lines 46-57].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Li [U.S. Patent Application Publication #2004/0126672 A1] discloses process modeling. Sonderman et al. [U.S. Patent Application Publication #2004/0121495 A1] disclose a model unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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